IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 8. This sheet, which includes Figs. 8 and 9, replaces the original sheet including Figs. 8 and 9.

Attachment: Replacement Sheet (1)

REMARKS/ARGUMENTS

Favorable reconsideration of this application, in view of the present amendments and in light of the following discussion, is respectfully requested.

Claims 9-20 are pending. Claims 9, 12-14 and 19-20 are amended to further clarify the features contained therein. No new matter is introduced.

In the outstanding Office Action, Figure 8 was objected to; Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the background in view of Feld (U.S. Patent No. 6,281,755, hereafter "Feld"); Claims 1, 10 and 17-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the background in view of Feld and Kaczynski (U.S. Patent Application Publication No. 2007/0111684); Claims 12-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the background in view of Feld and Shohara (U.S. Patent Application Publication No. 2005/0078743); Claim 14 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the background in view of Kasuga (U.S. Patent No. 4,524,422); Claims 15-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the background in view of Feld, Kasuga and Daners (U.S. Patent No. 6,229,393); and Claims 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the background in view of Kasuga and Shohara.

Initially, the replacement sheet of drawings submitted herewith includes amendments to Figure 8 addressing the informalities identified in the outstanding Office Action.

Accordingly, it is respectfully requested that the objection to Figure 8 be withdrawn.

Turning to the rejection of Claim 9 as being unpatentable over the background in view of Feld, Claim 9 is amended to recite, *inter alia*, an amplifier that includes:

an amplification device, an output terminal of the amplification device being an output terminal of the amplifier, a load to the amplifier being directly coupled to the amplification device; Application No. 10/580,645 Reply to Office Action of July 29, 2009

an LC parallel resonant circuit connected in parallel to the amplification device; and

an LCR series resonant circuit connected in parallel to the amplification device and the LC parallel resonant circuit.

Turning to the applied references, <u>Feld</u> describes a high-frequency narrow-band amplifier that feeds an antenna of a nuclear magnetic resonance tomography apparatus. ¹ <u>Feld</u> illustrates an output matching network (8) connected in series between an amplifier stage (2) of the power amplifier and a load impedance (G_L) thereof. ² <u>Feld</u> also describes that the output matching network (8) transforms the output impedance value (G_L) to a lower impedance value (G_L) seen by the amplifier stage (2) to allow proper feeding of the antenna. ³

However, Feld does not describe that the load (G_L) is directly coupled to the amplifier stage (2). Instead, Feld clearly illustrates that the load (G_L) is coupled to the output of the amplifier stage (2) through inductor (L_s) and capacitor (C_s) .⁴ In fact, Feld teaches away from directly coupling load (G_L) to the amplifier stage (2) insofar as Feld states that capacitance (C_s) is necessary to separate DC voltages from the antenna to ensure electrical safety.⁵ Conversely, amended Claim 9 recites that a load to the amplifier is directly coupled to the amplification device. Therefore, Feld fails to disclose the claimed amplification device.

Moreover, the outstanding Office Action combines <u>Feld</u> with the background in rejecting Claim 9. The outstanding Office Action asserts that the background describes an output terminal of the amplification device being an output terminal of the amplifier. However, as discussed above, <u>Feld</u> teaches away from a direct connection between an amplification device and an output terminal, or a load connected thereto insofar as <u>Feld</u> requires a series capacitor between the amplification device and the output terminal to block

¹ Feld at column 2, lines 55-60.

² Feld at column 5, lines 40-60; see also Figure 2.

³ Id.

⁴ See Figure 5 of <u>Feld</u>.

⁵ Feld at column 7, lines 44-47.

⁶ See the outstanding Office Action at pages 3-4.

DC voltage and increase electrical safety.⁷ Therefore, <u>Feld</u> teaches away from the combination of the background and <u>Feld</u>, and amended Claim 9 is believed to be in condition for allowance. Accordingly, it is respectfully requested that the rejection of Claim 9 under 35 U.S.C. § 103(a) be withdrawn.

As to the rejection of Claim 14 as being unpatentable over the background in view of Kasuga, Claim 14 is amended to recite, *inter alia*, an amplifier that includes:

an amplification device, an output terminal of the amplification device being an output terminal of the amplifier, a load to the amplifier being directly coupled to the amplification device; and

an analog band-pass filter connected in parallel to the output terminal of the amplification device, the analog band-pass filter having a plurality of poles provided on a left side of an s-plane and a plurality of zeros arranged between the poles, at least two zeros being arranged at locations other than an origin of the splane.

The background describes a wide-band amplifier that includes an inductor, capacitor and resistor connected in parallel to an amplifier device. However, the background describes that this filter does not have a flat pass band over a wide band width and has an unacceptable group delay time. The background also describes that the wide-band amplifier described therein has a single zero located at the origin of the s-plane and two poles located at positions other than the origin of the s-plane. However, as acknowledged by the outstanding Office Action, the background does not describe a plurality of zeroes arranged between the poles where at least two zeroes are arranged at locations other than the origin of the s-plane. To remedy this deficiency in the background, the outstanding Office Action combines the background with Kasuga.

⁸ See paragraph [0010] and Figure 8.

⁷ Feld at column 7, lines 43-47.

⁹ See the specification at paragraphs [0017]-[0018].

¹⁰ See, e.g., the specification at page 5; and Figure 9.

¹¹ See the outstanding Office Action at pages 3-4.

Kasuga describes a *digital* equalizer having poles and zeroes arranged along the circumference of a circle whose radius is the center angular frequency of a filter characteristic of the equalizer.¹² More specifically, Kasuga describes that an analog signal is digitized and held in register (21) from which samples are successively applied to delay devices (22, 23) in a cascade direction and delayed by a sampling period (T).¹³ The outputs of register (21), delays (22, 23) and delays (30, 31) are time division multiplexed into multiplier (25) and then summed with a previous output sample stored in register (28) by adder (27).¹⁴ The output of the equalizer (29) is then fed back to delay (30).¹⁵ Therefore, Kasuga merely describes a digital filter whose poles and zeroes are generated using a register delay line, multiplier and adder.

Therefore, any combination of the background with <u>Kasuga</u> will require more than a simple substitution of the pole-zero response of the digital filter in <u>Kasuga</u> with the pole-zero response of the analog circuit of the background. In fact, such a substitution will require a complete change in the principle of operation of the circuit described in the background as the suggested combination would require a substantial reconstruction and redesign of the analog circuit shown in Figure 8 of the background to include at least register (21), delays (22, 23, 30, 31) multiplier (25) adder (27) and register (28) described in <u>Kasuga</u>.

Furthermore, such a redesign would necessarily change the basic principle under which the analog circuit in Figure 8 of the background was designed to operate.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

¹² Kasuga at column 1, lines 43-50.

¹³ Kasuga at column 12, lines 40-51.

¹⁴ Kasuga at column 12, lines 52-61.

¹⁵ Kasuga at column 12, lines 60-67.

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Thus, based on the discussion above, it is submitted that the combination of the

background with Kasuga is improper, and that the outstanding Office Action fails to make a

prima facie case of obviousness with regard to Claim 14. As such, it is believed that Claim

14 is in condition for allowance, and it is respectfully requested that the rejection of Claim 14

under 35 U.S.C. § 103(a) be withdrawn.

As the rejection of Claims 10, 11, 12, 13, 17 and 18 rely upon Feld for describing the

above-distinguished features, and Feld does not disclose or suggest the above-distinguished

features, alone or in combination with any other art of record, it is respectfully requested that

the rejection of Claims 10-13 and 17-18 under 35 U.S.C. § 103(a) be withdrawn.

Further, as the rejection of Claims 15-16 and 19-20 rely upon the combination of the

background with Kasuga, and for the reasons discussed above, the combination of the

background and Kasuga is improper, it is submitted that a prima facie case of obviousness

has not been presented. Accordingly, it is respectfully requested that the rejection of Claims

15-16 and 19-20 under 35 U.S.C. § 103(a) be withdrawn.

For the reasons discussed above, no further issues are believed to be outstanding in

the present application, and the present application is believed to be in condition for formal

allowance. Therefore, a Notice of Allowance for Claims 9-20 is earnestly solicited.

Respectfully submitted,

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